AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Original) An optical receiver for receiving a first input data signal and a second input data signal, the optical receiver comprising:

a) a first photo-detector, the first photo-detector operable to receive the first input data signal and operable to output a first electrical signal;

b) a phase-locked-loop, the phase-locked-loop operable to receive a reference clock signal;

c) a clock-recovery circuit, the clock-recovery circuit coupled to the phase-locked-loop, the clock-recovery circuit operable to receive the first electrical signal;

d) a first latch-decision circuit, the first latch-decision circuit coupled to the clock-recovery circuit;

e) a first latch, the first latch coupled to the first latch-decision circuit, the first latch operable to receive the first electrical signal;

f) a second photo-detector, the second photo-detector operable to receive the second input data signal and operable to output a second electrical signal;

g) a second latch-decision circuit, the second latch-decision circuit coupled to the clock-recovery circuit; and

h) a second latch, the second latch coupled to the second latch-decision circuit, the second latch operable to receive the second electrical signal.

2. (Currently Amended) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the phase-locked-loop is operable to generate a

plurality of clock signals that have a frequency that is approximately equal to ~~higher than~~ the frequency of the reference clock signal.

3. (Currently Amended) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the phase-locked-loop is operable to generate a plurality of clock signals that have a frequency that is approximately equal to ~~higher than~~ the frequency of the reference clock signal and wherein at least one of the plurality of clock signals has a phase that is not equal to the phase of the reference clock signal.

4. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the clock-recovery circuit is operable to extract timing information from the first electrical signal.

5. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the first latch-decision circuit, based upon timing information received from the clock-recovery circuit, is operable to determine a time to latch the first electrical signal.

6. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the first latch-decision circuit is operable to receive the first electrical signal.

7. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the first latch-decision circuit is operable to receive the first electrical signal and the second latch-decision circuit is operable to receive the second electrical signal.

8. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the first latch-decision circuit is operable to receive the first electrical signal and, based upon information extracted from the first electrical signal and timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal.

9. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the first photo-detector includes a photo-diode.

10. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 1, wherein the first photo-detector is operable to receive an optical signal that is compliant with an optical signal defined in the InfiniBand specification.

11. (Original) An optical receiver for receiving a first input data signal and a second input data signal, the optical receiver comprising:

a) a first photo-detector, the first photo-detector operable to receive the first input data signal and operable to output a first electrical signal;

b) a phase-locked-loop, the phase-locked-loop operable to receive a reference clock signal;

c) a clock-recovery circuit, the clock-recovery circuit coupled to the phase-locked-loop, the clock-recovery circuit operable to receive the first electrical signal;

d) a latch-decision circuit, the latch-decision circuit coupled to the clock-recovery circuit;

e) a first latch, the first latch coupled to the latch-decision circuit, the first latch operable to receive the first electrical signal;

f) a second photo-detector, the second photo-detector operable to receive the second input data signal and operable to output a second electrical signal; and

g) a second latch, the second latch coupled to the latch-decision circuit, the second latch operable to receive the second electrical signal.

12. (Currently Amended) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the phase-locked-loop is operable to generate a plurality of clock signals that have a frequency that is approximately equal to ~~higher than~~ the frequency of the reference clock signal.

13. (Currently Amended) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the phase-locked-loop is operable to generate a plurality of clock signals that have a frequency that is approximately equal to ~~higher than~~ the frequency of the reference clock signal and wherein at least one of the plurality of clock signals has a phase that is not equal to the phase of the reference clock signal.

14. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the clock-recovery circuit is operable to extract timing

information from the first electrical signal.

15. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the latch-decision circuit, based upon timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal and the second input signal.

16. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the latch-decision circuit is operable to receive the first electrical signal.

17. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the first latch-decision circuit is operable to receive the first electrical signal and, based upon information extracted from the first electrical signal and timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal.

18. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the first photo-detector includes a photo-diode.

19. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 11, wherein the first photo-detector is operable to receive an optical signal

that is compliant with an optical signal defined in the InfiniBand specification.

20. (Original) An optical receiver for receiving a first input data signal and a second input data signal, the optical receiver comprising:

a) a first photo-detector, the first photo-detector operable to receive the first input data signal and operable to output a first electrical signal;

b) a second photo-detector, the second photo-detector operable to receive the second input data signal and operable to output a second electrical signal;

c) a phase-locked-loop, the phase-locked-loop operable to receive a reference clock signal;

d) a clock-recovery circuit, the clock-recovery circuit coupled to the phase-locked-loop, the clock-recovery circuit operable to receive the first electrical signal;

e) a latch-decision circuit, the latch-decision circuit coupled to the clock-recovery circuit; and

f) a latch, the latch coupled to the latch-decision circuit, the latch operable to receive the first electrical signal and the second electrical signal.

21. (Currently Amended) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the phase-locked-loop is operable to generate a plurality of clock signals that have a frequency that is approximately equal to ~~higher than~~ the frequency of the reference clock signal.

22. (Currently Amended) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the phase-locked-loop is operable to generate a

plurality of clock signals that have a frequency that is approximately equal to ~~higher than~~ the frequency of the reference clock signal and wherein at least one of the plurality of clock signals has a phase that is not equal to the phase of the reference clock signal.

23. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the clock-recovery circuit is operable to extract timing information from the first electrical signal.

24. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the latch-decision circuit, based upon timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal and the second input signal.

25. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the latch-decision circuit is operable to receive the first electrical signal.

26. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the first latch-decision circuit is operable to receive the first electrical signal and, based upon information extracted from the first electrical signal and timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal.

27. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the first photo-detector includes a photo-diode.

28. (Original) The optical receiver for receiving the first input data signal and the second input data signal of claim 20, wherein the first photo-detector is operable to receive an optical signal that is compliant with an optical signal defined in the InfiniBand specification.